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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,386	07/01/2003	Frank Lin	VIAP0090USA	9347

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EXAMINER

RUTZ, JARED IAN

ART UNIT PAPER NUMBER

2187

DATE MAILED: 08/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/609,386

Applicant(s)

LIN ET AL.

Examiner

Jared I. Rutz

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 01 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-40 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1,2,6,7,9-13,17,18,20-32,35-37 and 40 is/are rejected.
- 7) ☒ Claim(s) 3-5,8,14-16,19,33,34,38 and 39 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☒ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

Claims 1-40 as originally filed on 7/01/2003 are pending in the instant application. Of these there are 5 independent claims and 35 dependent claims.

#### ***Priority***

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Taiwan R.O.C. on 1/15/2003. It is noted, however, that applicant has not filed a certified copy of the 60/440,046 application as required by 35 U.S.C. 119(b).
2. It is believed by the examiner based on the specification that the application to which priority is being claimed is the US provisional application 60/440,046, and that the declaration inadvertently is referring to an application filed in Taiwan R.O.C. If this is the case, the applicant is required to submit a substitute declaration or oath to correct the deficiencies set forth above.

#### ***Specification***

1. The disclosure is objected to because of the following informalities:
  - a. Page 1 lines 24-25 reads "Personal computer systems and their associated are such data processing systems." Please clarify the meaning of "their associated".
  - b. Page 14 lines 3-4 reads "The read request RA2, therefore, is just pushed into the request queue 40." The examiner believes that "RA2" should be "RB2", as RA2 is already in the request queue.

2. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. **Claims 1, 2, 6, 7, 9-13, 17, 18, 20-29, 30-32, 35-37, and 40** are rejected under 35 U.S.C. 102(e) as being anticipated by Van Hook et al (US 6,564,304).

5. **Claim 1** is taught by Van Hook as:

c. A method for accessing a memory device of a computer system, the memory device being electrically connected to a memory controller. Column 3 lines 50-52.

d. The memory controller sequentially responding to a master device according to a sequence of access requests issued in order by the master device. Column 4 lines 32-34.

- e. The memory controller comprising a request queue. Column 4 lines 42-44.
  - f. And a latency monitoring unit electrically connected to the request queue. Column 4 lines 44-47.
  - g. The method comprising: (a) using the request queue to store access requests generated from the master device. Column 4 lines 42-44.
  - h. (b) Using the latency monitoring unit to record a plurality of latency values, the latency values respectively corresponding to the access requests stored in the request queue. Column 4 lines 39-41 shows that latency information is stored in the request cue.
  - i. (c) Using the memory controller to receive a first access request and add the first access request to the request queue with an associated queue priority according to latency values associated with the access requests already stored in the request queue. See column 5 lines 54-55, which shows that the reordering takes the latency into account.
  - j. And (d) using the memory controller to sequentially access the memory device according to the associated queue priorities of the access requests stored in the request queue. Column 5 lines 64-65 show that the requests are executed in the selected order.
6. **Claim 2** is taught by Van Hook as:
- k. The method of claim 1 wherein step (c) further comprises: determining that the first access request is used to access a first page of the memory device.

Column 3 lines 54-55 show that the instructions are reordered so that page switches are minimized, therefore it is inherent that the page accessed is determined.

- I. And determining if a second access request used to access the first page of the memory device and a third access request used to access a second page of the memory device have been stored in the request queue, the third access request immediately following the second access request and having a queue priority lower than a queue priority of the second access request. The sort queue determines which banks of memory are accessed by each request as part of its sorting algorithm so that page switches are minimized (column 3 lines 54-55).
7. **Claim 6** is taught by Van Hook as:
  - m. The method of claim 2 wherein step (c) further comprises: if the second access request stored in the request queue corresponds to a lowest queue priority, adding the first access request to the request queue with the lowest queue priority, and assigning an initial value to a first latency value corresponding to the first access request. Column 5 lines 12-14 show that the latency requirements are taken into account as well as the bank switching. The only way to insert the first access request that takes bank switching and latency into account is after the second access request. Column 4 lines 39-41 show that latency requirements are provided to the request queue, which would be an initial value for the latency.
8. **Claim 7** is taught by Van Hook as:

- n. The method of claim 2 wherein step (c) further comprises: if the request queue is empty, adding the first access request to the request queue, and assigning an initial value to a first latency value corresponding to the first access request. Column 4 lines 63-65 states that the requests are provided to the sort queue. Column 4 lines 39-41 show that latency requirements are provided to the request queue, which would be an initial value for the latency.
9. **Claim 9** is taught by Van Hook as:
- o. The method of claim 1 wherein the memory device is a main memory of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture.
10. **Claim 10** is taught by Van Hook as:
- p. The method of claim 9 wherein the main memory is dynamic random access memory (DRAM). Column 5 lines 21-22.
11. **Claim 11** is taught by Van Hook as:
- q. The method of claim 1 wherein the memory controller is positioned within a north bridge circuit of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture. This type of memory controller is referred to as a northbridge in the art. A northbridge definition from Whatis.com is cited as a supporting reference.
12. **Claim 12** is taught by Van Hook as:

- r. A method of accessing a memory device of a computer system through a memory controller. Column 3 lines 50-52.
  - s. The memory controller sequentially responding to a master device according to a sequence of access requests issued in order by the master device. Column 4 lines 32-34.
  - t. The method comprising: (a) storing access requests generated from the master device in a request queue; Column 4 lines 42-44.
  - u. (b) recording a plurality of latency values, the latency values respectively corresponding to the access requests stored in the request queue. Column 4 lines 39-41 shows that latency information is stored in the request cue.
  - v. (c) receiving a first access request and adding the first access request to the request queue with an associated queue priority according to latency values associated with the access requests already stored in the request queue. See column 5 lines 54-55, which shows that the reordering takes the latency into account.
  - w. And (d) sequentially accessing the memory device according to the associated queue priorities of the access requests stored in the request queue. Column 5 lines 64-65 show that the requests are executed in the selected order.
13. **Claim 13** is taught by Van Hook as:
- x. The method of claim 12 wherein step (c) further comprises: determining that the first access request is used to access a first page of the memory device. Column 3 lines 54-55 show that the instructions are reordered so that page



switches are minimized, therefore it is inherent that the page accessed is determined.

y. And determining if a second access request used to access the first page of the memory device and a third access request used to access a second page of the memory device have been stored in the request queue, the third access request immediately following the second access request and having a queue priority lower than a queue priority of the second access request. The sort queue determines which banks of memory are accessed by each request as part of its sorting algorithm so that page switches are minimized (column 3 lines 54-55).

14. **Claim 17** is taught by Van Hook as:

z. The method of claim 2 wherein step (c) further comprises: if the second access request stored in the request queue corresponds to a lowest queue priority, adding the first access request to the request queue with the lowest queue priority, and assigning an initial value to a first latency value corresponding to the first access request. Column 5 lines 12-14 show that the latency requirements are taken into account as well as the bank switching. The only way to insert the first access request that takes bank switching and latency into account is after the second access request. Column 4 lines 39-41 show that latency requirements are provided to the request queue, which would be an initial value for the latency.

15. **Claim 18** is taught by Van Hook as:

- aa. The method of claim 13 wherein step (c) further comprises: if the request queue is empty, adding the first access request to the request queue, and assigning an initial value to a first latency value corresponding to the first access request. Column 4 lines 63-65 states that the requests are provided to the sort queue. Column 4 lines 39-41 show that latency requirements are provided to the request queue, which would be an initial value for the latency.
16. **Claim 20** is taught by Van Hook as:
- bb. The method of claim 1 wherein the memory device is a main memory of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture.
17. **Claim 21** is taught by Van Hook as:
- cc. The method of claim 9 wherein the main memory is dynamic random access memory (DRAM). Column 5 lines 21-22.
18. **Claim 22** is taught by Van Hook as:
- dd. The method of claim 1 wherein the memory controller is positioned within a north bridge circuit of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture. This type of memory controller is referred to as a northbridge in the art. A northbridge definition from Whatis.com is cited as a supporting reference.
19. **Claim 23** is taught by Van Hook as:

- ee. A memory controller for accessing a memory device of a computer system, the memory device being electrically connected to a memory controller, the memory controller sequentially responding to a master device according to a sequence of access requests issued in order by the master device. Column 4 lines 32-34
  - ff. The memory controller comprising: a request queue for storing access requests generated from the master device. Column 4 lines 42-44.
  - gg. A latency monitoring unit electrically connected to the request queue for recording a plurality of latency values, the latency values respectively corresponding to the access requests stored in the request queue. Column 4 lines 39-41 shows that latency information is stored in the request cue.
  - hh. And a reorder decision-making unit electrically connected to the request queue for controlling a first access request added to the request queue with an associated queue priority according to latency values associated with the access requests already stored in the request queue. Column 4 lines 44-47 shows that an arbitrator decides the how to order the memory requests. Column 5 lines 54-55 shows that the latency is taken into account.
  - ii. Wherein the memory device is sequentially accessed according to the associated queue priorities of the access requests stored in the request queue. Column 5 lines 64-65 show that the requests are executed in the selected order.
20. **Claim 24** is taught by Van Hook as:

jj. The memory controller of claim 23 further comprises: a page/bank comparing unit electrically connected to the reorder decision-making unit and the request queue for determining that the first access request is used to access a first page of the memory device and determining if a second access request used to access the first page of the memory device and a third access request used to access a second page of the memory device have been stored in the request queue, wherein the third access request immediately follows the second access request and has a queue priority lower than a queue priority of the second access request. The sort queue determines which banks of memory are accessed by each request as part of its sorting algorithm so that page switches are minimized (column 3 lines 54-55).

21. **Claim 25** is taught by Van Hook as:

kk. The memory controller of claim 24 further-comprising: a latency control unit electrically connected to the reorder decision-making unit and the latency monitoring unit for detecting whether a third latency value corresponding to the third access request is greater than a maximum allowance value. Column 3 line 66 to column 4 line 3 shows that latency requirements are considered when requests are reordered. This shows that a reorder will not be made if it prevents a request from meeting its latency requirements.

22. **Claim 26** is taught by Van Hook as:

- II. The memory controller of claim 25 wherein the maximum allowance value is programmable. The latency value is programmed by the master that makes the access request (column 4 lines 39-41).
23. **Claim 27** is taught by Van Hook as:
- mm. The method of claim 1 wherein the memory device is a main memory of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture.
24. **Claim 28** is taught by Van Hook as:
- nn. The method of claim 9 wherein the main memory is dynamic random access memory (DRAM). Column 5 lines 21-22.
25. **Claim 29** is taught by Van Hook as:
- oo. The method of claim 1 wherein the memory controller is positioned within a north bridge circuit of the computer system. Column 3 lines 56-58 state that the memory request controller is provided in a combined CPU and graphics processing architecture. This type of memory controller is referred to as a northbridge in the art. A northbridge definition from Whatis.com is cited as a supporting reference.
26. **Claim 30** is taught by Van Hook as:
- pp. A method for accessing a memory device of a computer system, the method comprising: receiving one or more access requests for accessing the memory device in a first predetermined order; and reordering the access requests in a second predetermined order to be processed in a request queue by

relocating a first access request to follow a second access request accessing a same memory page. Column 3 lines 54-55 show that requests are reordered to minimize page switches. In order to reorder, there must be a first predetermined order that is reordered to provide a second predetermined order.

qq. Wherein the relocating is prohibited if it increases a processing latency for a third access request to exceed a predetermined limit. Column 3 line 66 to column 4 line 3 shows that latency requirements are considered when requests are reordered. This shows that a reorder will not be made if it prevents a request from meeting its latency requirements.

27. **Claim 31** is taught by Van Hook as:

rr. The method of claim 30 wherein the third access request immediately follows the second access request in the request queue before the first access request is inserted. Using the definitions of second and first access requests as given in claim 2 “the third access request immediately following the second access request and having a queue priority lower than a queue priority of the second access request” this is inherent in the stated claim.

28. **Claim 32** is taught by Van Hook as:

ss. The method of claim 30 wherein the reordering further includes: identifying that the first and the second access requests access the same memory page; determining that the third access request is for accessing a different memory page. The sort queue determines which banks of memory are accessed by

each request as part of its sorting algorithm so that page switches are minimized (column 3 lines 54-55).

tt. And inserting the first access request between the second and the third access requests in the request queue. Column 3 lines 54-55 state that instructions are reordered so that page switches are reordered. Column 5 lines 12-14 show that the latency requirements are taken into account as well as the bank switching. The only way to insert the first access request that takes bank switching and latency into account is between the second and third access requests.

29. **Claim 35** is taught by Van Hook as:

uu. The method of claim 30 wherein the maximum latency value is programmable. The latency value is programmed by the master that makes the access request (column 4 lines 39-41).

30. **Claim 36** is taught by Van Hook as:

vv. A method for accessing a memory device of a computer system, the method comprising: receiving one or more access requests for accessing the memory device, the access requests accessing one or more memory pages; and arranging the access requests in a predetermined order to be processed in a request queue by putting one or more access requests together for accessing a same memory page consecutively in one or more groups. Column 3 lines 54-55.

ww. Wherein an access request is prohibited from being grouped to be processed before at least one other access request if the grouping increases a

processing latency of the at least one other access request in the request queue to exceed a predetermined limit. The memory controller takes into account the latency requirements of the memory requests (column3 line 66 to column 4 line 3.)

31. **Claim 37** is taught by Van Hook as:

xx. The method of claim 36 wherein the arranging further includes: identifying that a first access request received after a second access request accesses the same memory page as the second access request; determining that a third access request is for accessing a different memory page; inserting the first access request between the second and the third access requests in the request queue; and repeating the above identifying, determining and inserting steps for all received access requests. Column 3 lines 54-55 state that instructions are reordered so that page switches are reordered. Column 5 lines 12-14 show that the latency requirements are taken into account as well as the bank switching. The only way to insert the first access request that takes bank switching and latency into account is between the second and third access requests.

32. **Claim 40** is taught by Van Hook as:

yy. The method of claim 36 wherein the maximum latency value is programmable. The latency value is programmed by the master that makes the access request (column 4 lines 39-41).



***Allowable Subject Matter***

33. **Claims 3-5, 8, 14-16, 19, 33-34, and 38-39** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

34. **Claims 3 and 14** recite the limitation "increasing the third latency value by a predetermined increment value". Although the invention disclosed by Van Hook considers the latency requirements of a memory access request, it does not disclose changing the latency value associated with a request to reflect the change in the latency due to a reorder.

35. **Claims 4-5 and 15-16** depend on the instant claims and are allowable for the reasons discussed supra with respect to claims 3 and 14.

36. With respect to **claims 8 and 19**, the record is clear as to the reasons for allowability.

37. **Claims 33 and 38** recite the "limitations examining whether the latency value associated with the third access request is increased to exceed the predetermined limit if the first access request is to be inserted" and "increasing the latency value associated with the third access request by a predetermined incremental value if the first access request is inserted." These steps are not taught by Van Hook.

38. **Claims 34 and 39** depend on the instant claims and are allowable for the reasons discussed supra with respect to claims 33 and 38.

**Conclusion**

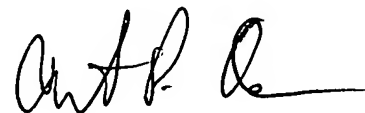
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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